REMARKS

The Office Action mailed December 20, 2004 has been carefully reviewed and the forgoing amendment and following remarks are made in consequence thereof.

Claims 1, 3, 5, 6, and 26-30 are pending in this application. Claims 1, 3, 5, 6, and 26-30 are rejected. Claims 2, 4, and 7-25 have been canceled.

Preliminarily, Applicants thank Examiner for courtesies extended to Applicants' representative during a telephonic interview conducted on January 6, 2005, during which the section 112 rejections of the present Office Action were discussed. No agreement was reached on the claims.

Applicants traverse the assertion in the Advisory Action that amending Claim1 from "initiating a predetermined time delay" to "initiating a predetermined time delay greater than zero time" appears to be new matter. Specifically, any time delay requires a delay greater than zero time. A time delay of less than zero time is impossible in that it implies that an event occurs before the initiating event can occur. A time delay equal to zero time is not a delay. A phrase "time delay," having a meaning a delay of greater than zero time is entirely consistent with the ordinary meaning of time delay, as would be understood by one of ordinary skill in the art at the time the application was filed. Accordingly, applicants respectfully submit that qualifying "time delay" with the phrase "greater than zero time" does not add new matter.

Applicants respectfully submit that initiating a predetermined time delay greater than zero time is fully supported in the originally filed specification at least in Figure 3. Specifically, pulse output timer 140 is illustrated with an exemplary ten second delay, pulse output timer 142 is illustrated with an exemplary one second delay, and delay initiation timer 150 is illustrated with an exemplary two second delay.

The rejection of Claims 1, 3, 5, 6, and 26-30 under 35 U.S.C. § 112, first paragraph is respectfully traversed. Claims 1 and 26 have each been amended to indicate that the claimed time delay is a time delay that is greater than a zero time delay and to indicate that during the initiated time delay the selected operating mode is reset. Specifically, Claim 1 recites, "operating the system in a first operating mode, the first operating mode comprising a predetermined configuration of valves, dampers, motors, and pumps," which is described in

the specification at Paragraph [0023], lines 5-6 as "mode describes a pre-determined system 4 configuration of such typical system components, including, but not limited to, valves, dampers, motors, and pumps." Claim 1 further recites, "selecting a second operating mode to switch the system operation to," which is described in the specification at Paragraph [0023], lines 2-4 as "an operator selects a desired operational mode to change system 4 current configuration to a pre-determined configuration, such as, but not limited to a Mode One, a Mode Two, and a standby mode." Claim 1 also recites, "receiving a signal indicative of the system meeting permissive requirements for entering the selected mode," which is described in the specification at Paragraph [0024], lines 11-12 as "logic mode 102 also determines whether the pre-determined permissives have been met." Claim 1 further recites, "initiating a predetermined time delay greater than zero time," which is described in the specification at Paragraph [0024], lines 17-20 as "[w]hen first mode initiate switch 112 is initialized, first mode initiate switch 112 output and AND gate 128 output are "ANDED" by AND gate 130 which is then output to pulse output timer 142 and pulse output timer 144." Claim 1 further recites, "resetting the selected operating mode during the time delay," which is described in the specification:

> pulse output timer 142, pulse output timer 144, and delay initiation timer 150 allow the mode to be reset. Additionally, timer 144, in conjunction with flip-flop 160, allow multiple mode resets, i.e. timer 144 holds flip-flop 160 in the set-override position until other modes, i.e. mode 2 initiate signal input from OR gate 124, are reset which drops out the reset command to the selected mode, i.e. Mode 1.

Paragraph [0025], lines 1-7. Claim 1 further recites, "switching the system to a second operating mode without going to a standby mode, the second operating mode comprising a predetermined configuration of valves, dampers, motors, and pumps different than the first mode, and wherein at least one of the valves, dampers, motors, or pumps is positioned to a different operating position in the second operating mode than that respective valve, damper, motor, or pump was positioned for operation during the first operating mode," which is described in the specification:

> pulse output timer 144 includes a delay time which is greater than pulse output timer 142 delay time. Flip-flop 160 output is then used to actuate at least one pre-determined system 4 component from a first position or state to a second position or state. Pulse output timer 150 then drops out to allow the operator to either re-initialize Mode 1 or switch to another mode such as Mode 2 without going to a standby mode.

Paragraph [0025], lines 9-14. Additionally, Figure 3 illustrates an embodiment of the present invention wherein exemplary time delays associated with the various circuit components are shown within the graphic representing the component. Specifically, pulse output timer 140 includes a time delay of ten seconds, pulse output timer 142 includes a time delay of one second, pulse output timer 144 includes a time delay of ten seconds, and delay initiation timer 150 includes a time delay of two seconds.

Applicants respectfully traverse the assertion in the Office Action dated 7/13/2004 and incorporated by reference to the present Office Action dated 12/20/2004 that:

> "[b]ased on the claim language "resetting of the plurality of operating modes during the time delay" there is no support for switching from a first mode to a second mode of operation. That is if all conditions are reset, then the indicative signal causing the permissive requirement is reset. Thus the condition would no longer exist. Switching from a first mode to a second mode need not be done as the condition requiring such has been cleared. Furthermore there is no reason why the system could not be switched or retained in the first mode if the conditions are reset.

Firstly, the claim recites that the operating mode is reset, not "all conditions" as stated in the Office Action. Further, resetting the operating mode does not reset an indicative signal causing the permissive requirement. The permissive is illustrated in Figure 3 and described in the specification as an input to the logic and is not described as being reset when the operating mode is reset. For example, the specification recites:

> logic mode 102 also determines whether the pre-determined permissives have been met. If the pre-determined permissives for the Mode One have been met, then a signal is input to AND gate 126 and "ANDED" with OR gate 120 output. Alternatively, if the pre-determined permissives for Mode One have not been met then no signal is input to AND gate 126. AND gate 126 output and timer 140 output are input to AND gate 128 which is then output to AND gate 130.

Paragraph [0024], lines 11-16. The Office Action further states that "[s]witching from a first mode to a second mode need not be done as the condition requiring such has been cleared." The specification does not describe nor claim that any condition requires switching from a first mode to a second mode and that clearing the condition makes switching from a first mode to a second mode not needed.

Accordingly, Applicants respectfully submit that Claims 1, 3, 5, 6, and 26-30 meet the requirements of section 112 first paragraph. For at least the reasons set forth above, Applicants respectfully request the rejection to Claims 1, 3, 5, 6, and 26-30 under section 112, first paragraph be withdrawn.

The rejection of Claims 1, 3, 5, 6, and 26-30 under 35 U.S.C. § 112, second paragraph is respectfully traversed. Claims 1 and 26 have each been amended to indicate that the claimed time delay is a time delay that is greater than a zero time delay and to indicate that during the initiated time delay the selected operating mode is reset.. As described above, no residual condition need be present for the operating modes to be switched during the time delay. Claim 1 recites, "initiating a predetermined time delay greater than zero time," which is described in the specification at Paragraph [0024], lines 17-20 as "[w]hen first mode initiate switch 112 is initialized, first mode initiate switch 112 output and AND gate 128 output are "ANDED" by AND gate 130 which is then output to pulse output timer 142 and pulse output timer 144." As such initiating the time delay provides the change in logic state that causes the resetting of the selected operating mode during the time delay. Applicants traverse the assertion in the Office Action that "in order for the operating modes to be switched during reset some residual condition must be present to allow the switching of the modes." The specification and claims do not describe that the operating mode is switched

during reset, but rather the selected operating mode is reset during the time delay. Additionally, the "reason" for switching modes is not is not described nor claimed in the specification or claims and is not dependant on whether a condition or indicative signal exists.

Accordingly, Applicants respectfully submit that Claims 1, 3, 5, 6, and 26-30 meet the requirements of section 112 second paragraph. For at least the reasons set forth above, Applicant requests the Section 112, second paragraph, rejections of Claims 1, 3, 5, 6, and 26-30 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,

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